

PATENT APPLICATION  
DOCKET NO.: 1263-0025US

**REMARKS**

Claims 1-36 were originally presented for examination. Claims 1-8, 14, 15, 24, 25, 31, and 33 have been canceled without prejudice or limitation.

Claims 9, 19, 29, and 32 have been amended.

New claims 37-44 are added.

Claims 9-13, 16-23, 26-30, 32, 34-44 are currently pending. Claims 9, 19, 29, and 37 are in independent form.

No new matter is introduced hereby.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

**Regarding the Election/Restriction**

Responsive to the comments in the pending Office Action regarding the election and restriction requirement, Applicant hereby affirms the election to prosecute the invention of Group II comprising claims 9-36.

**Regarding the Claim Objections and Allowable Subject Matter**

Applicant appreciates the indication in the pending Office Action that claims 15, 25, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if

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rewritten in independent form. Applicant has amended the base claims 9, 19, and 29 by incorporating the allowable subject matter. Accordingly, it is believed that claims 9-13, 16-23, 26-30, 32, and 34-36 are in condition for allowance.

**Regarding the Claim Rejections - 35 U.S.C. §103(a)**

In the pending Office Action, claims 9-36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,515,593 to Bhavnagarwala (hereinafter the *Bhavnagarwala* reference) in view of U.S. Patent Application Publication No. 2003/0081492 in the names of Farrell et al. (hereinafter the *Farrell* reference). In connection with these rejections, the Examiner has commented as follows with respect to base claim 9:

Regarding independent claim 9, Fig. 3 of Bhavnagarwala discloses a Static Random Access Memory (SRAM) instance, comprising:

A plurality of SRAM cells organized in an array having rows and columns (Col. 1 line 32), each SRAM cell including a pair of cross-coupled inverters [306 and 302] that are coupled to form a pair of data nodes [314 and 316], wherein pull-down devices of said SRAM cells [302] forming a row are coupled together to be biased by a bias potential in standby mode ([SL] by control line 322);

However, Bhavnagarwala fails to disclose a row decoder and a multiplexer.

Fig. 2 of Farrell discloses a row decoder [130] for selectively activating wordlines based on a decoded address [A0-A12], wherein each wordline is operable to drive a corresponding row of said array [116 and 118]

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(Page 2, paragraph [0017]); and a multiplexer [124 and 126] disposed between said row decoder [130] and said array [116 and 118] for deactivating said bias potential provided to said SRAM cells of a particular row when said particular row is driven by a wordline associated therewith (see Fig. 2).

It would have been obvious to incorporate the structure of a row decoder and multiplexer as disclosed in Farrell into the SRAM cells as disclosed in Bhavnagarwala. One having the ordinary skill in the art would have been motivated to do this for the purpose of providing selection between memory cell for each memory arrays and memory cell within selected memory array.

Similar comments were also made with respect to base claim 19.

Regarding base claim 29, the following comments were provided:

Regarding independent claim 29, fig. 3 of Bhavnagarwala discloses a memory operation method associated with a Static Random Access Memory (SRAM) instance, said SRAM instance having a plurality of SRAM memory cells organized in an array having rows and columns (Col. 1 line 32), each SRAM cell including a pair of cross-coupled inverters [306 and 302] that are coupled to form a pair of data nodes [314 and 316], comprising:

in standby mode [SL], providing a bias potential to pull-down devices [302] of said SRAM cells that form a row of said array;

selectively activating a wordline [WL] based on a decoded address for a memory read operation; said wordline for accessing a bitcell on a row of SRAM cells (Col. 4 lines 60-65); and responsive to activating said wordline, deactivating said bias potential from said pull-down devices [302] of said row of SRAM cells [300] (col. 5 lines 5-10 mention that during read access, in which a row of wordline address/decoded must be well-known, the source line having the bias potential is maintained. Therefore, it would have been to one skill in the art that the bias potential from the source line

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*must be down or deactivate after the read access operation).*

Further, claims 14 and 24 are also rejected under 35 U.S.C. §103(a) as being unpatentable over the *Bhavnagarwala* and *Farrell* references as applied to base claims 9 and 19 above and in further view of U.S. Patent No. 6,920,060 to Chow et al.

Applicant respectfully submits that the pending §103(a) rejections as set forth above have been overcome or otherwise rendered moot by way of the present response. Applicant has amended the base claims 9, 19, and 29 wherein the subject matter indicated to be allowable has been incorporated. Accordingly, claims 9-13, 16-23, 26-30, 32, and 34-36 are believed to be allowable over the applied art of record.

**Regarding the New Claims**

Applicant has added new claims 37-44 by way of the present response, of which claim 37 is in independent form. As recited, base claim 37 is directed to a Static Random Access Memory (SRAM) circuit which comprises a plurality of bias switch elements, each corresponding to a wordline associated with a row of the SRAM array, each bias switch element comprising logic circuitry driven by a corresponding wordline to deactivate a bias potential applied

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to the source terminals of the SRAM cells when the corresponding wordline is driven high. As indicated in the pending Office Action, this feature is not anticipated or suggested in the applied art of record. Accordingly, the newly added claims 37-44 are also believed to be in condition for allowance.

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**CHARGE STATEMENT:**

It is believed that no fees are due with respect to this response. To the extent required, however, the Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fees(s) paid, or asserted to be filed, or which should have been filed herewith or concerning any paper filed as part of this transmittal to our **Deposit Account No. 03-1130.**

**This CHARGE STATEMENT does not authorize charge of the Issue Fee until/unless an Issue Fee transmittal form is filed.**

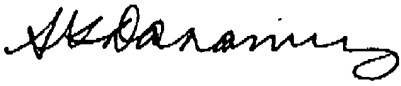
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**SUMMARY AND CONCLUSION**

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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